FE-I2 Status

K. Einsweiler, LBNL

According to previous schedule, chip should be submitted...

- Go through status of submission

Present estimate for submission date:

- PO for FE-I2 run is now ready for submission. Waiting for official quote for MCC-I2 run before starting PO process for this second submission.
- Working backwards from July SPS and PS beam dates suggests we must submit by Feb 18.
- Present best estimate is Feb 28.

Status of FE-I2 Work

Front-end:

- New front-end layout and verification is complete.
- The integration was much more difficult that expected, requiring almost 4 weeks to complete layout and wiring of the pixel front-end and control blocks.
- Without the sixth metal layer, this task would have been impossible.
- All items on our mandatory list were done. There was still enough room for one of the original three VDD decoupling capacitors.
- New circuit has been integrated for “auto-tuning” (late night initiative of Laurent and Ivan). This could shorten threshold tune time to less than 1 minute if it works...

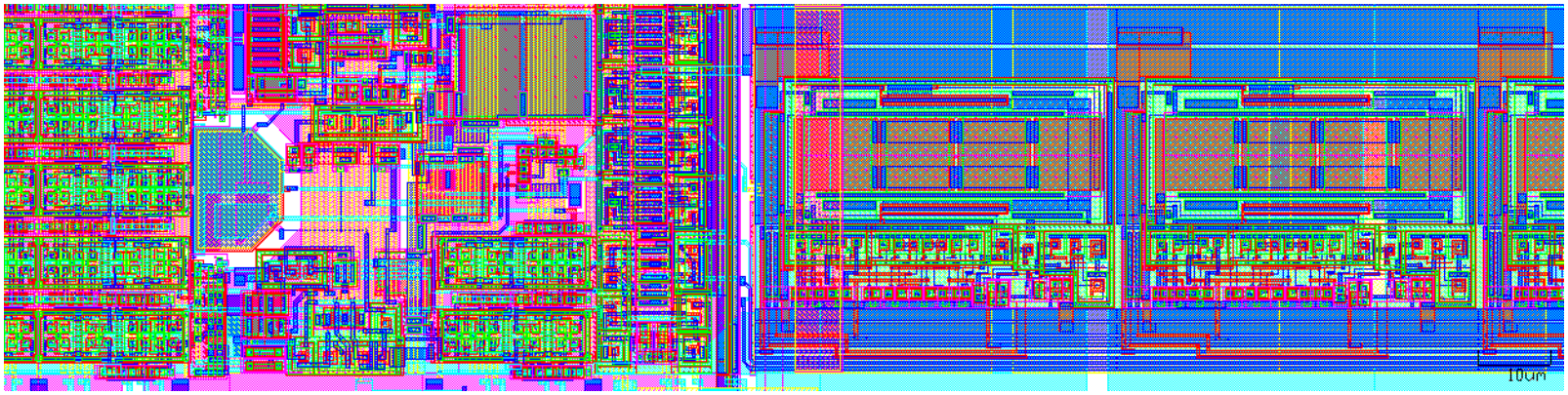
Front-end Integration:

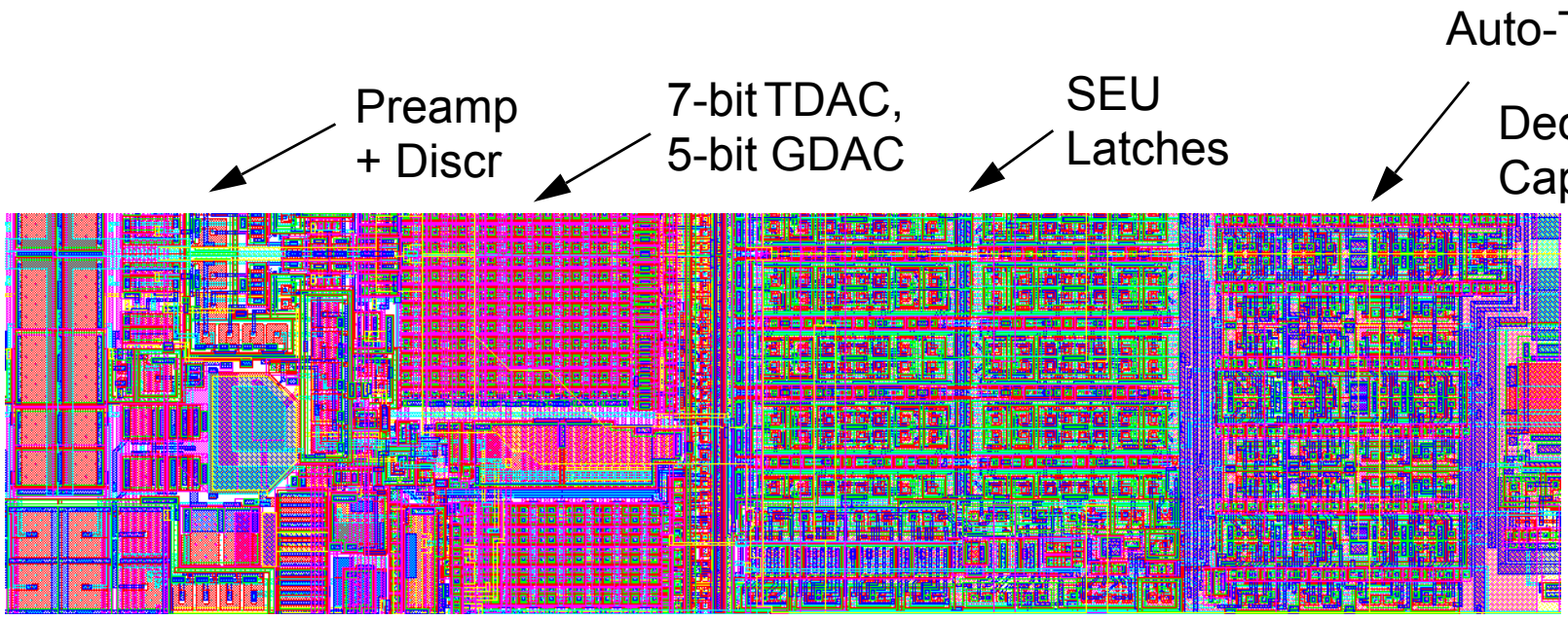
- All bussing of analog signals to the top and bottom of column busses has been completed. Several key signals were widened or better shielded.
- New circuitry has been integrated into the bottom of column region, including triple-redundant Global Register, 10-bit VCal DAC.

Column and Bottom of Column Integration:

- Now complete, with improvements in column readout speed and TOT processor speed, including parity generation for all hits. No changes to EOC buffer region.

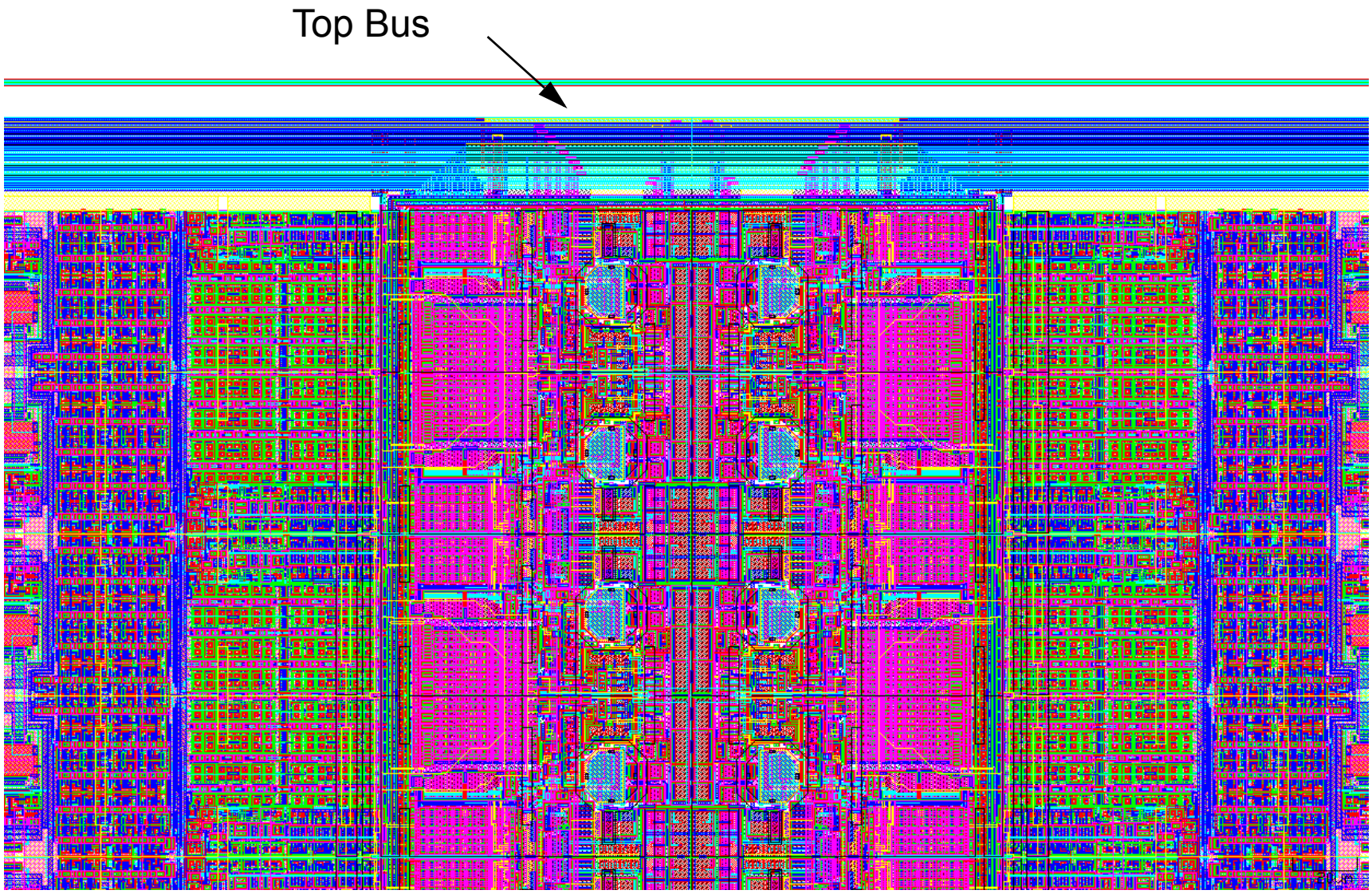
- Pixel front-end + control in FE-I1 was about 100μ long. In FE-I2, it is 200μ long.





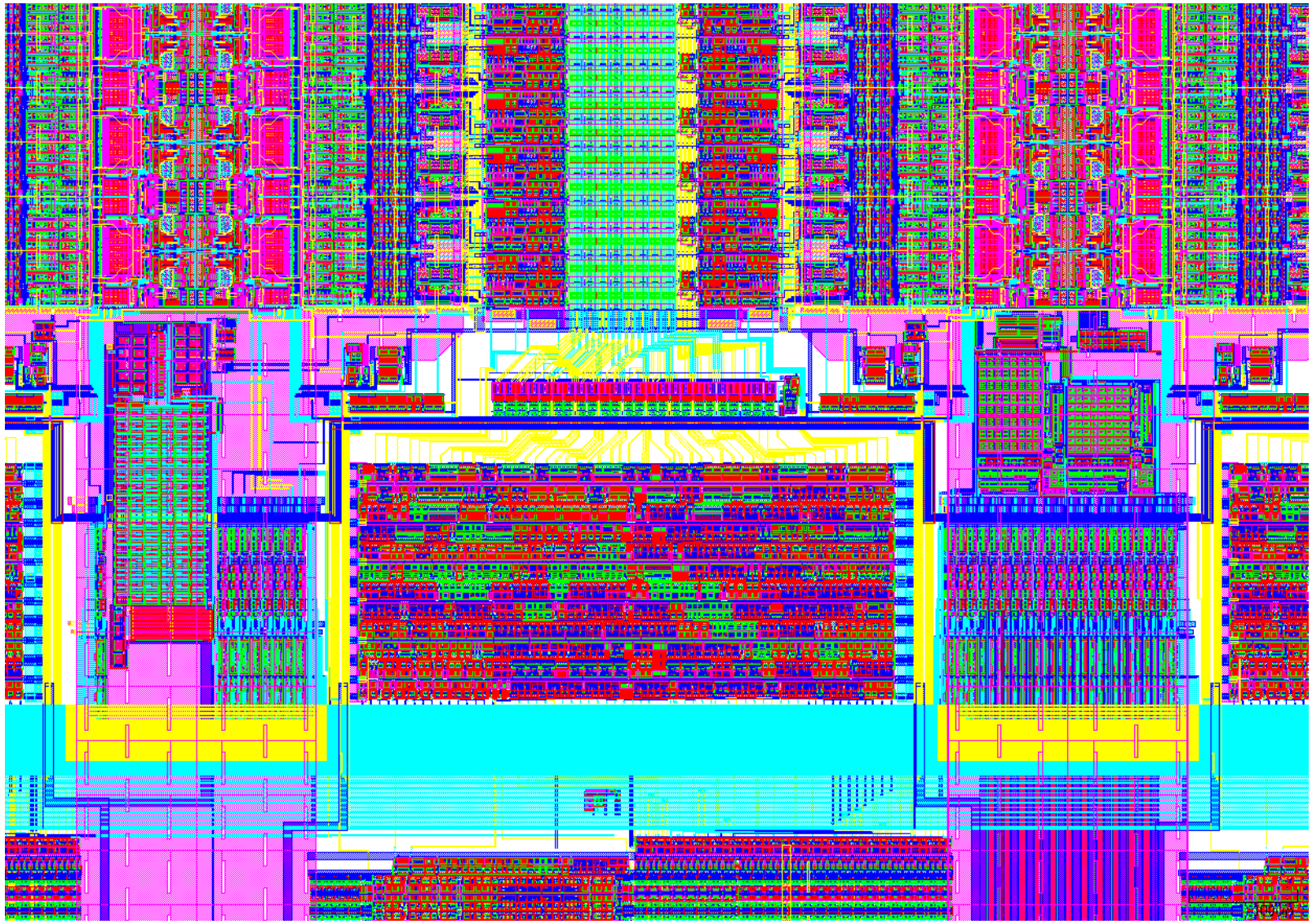
- New layout is extremely dense, and the floorplan is much cleaner.

- Integration into column pairs:



- Top bus integrates analog biassing and control without interference from fast digital signals. Sixth metal layer allowed implementing most new control signals here, leaving room for triple-redundant logic in the bottom of column region.

- Bottom of column region:



- New triple-redundant registers are much larger, despite compact layout. New TOT processor is roughly the same size. Bottom of column M2 bus now must jump up to M3 to cross over triple-redundant registers.

Remaining Work before Submission

Integration of bottom of chip:

- Integration of bottom of chip (supply busses and miscellaneous blocks plus completion of all top level schematics). This work is expected to be completed by Laurent by Feb 14.

Completion of updated Digital_Bottom block:

- The critical path at this point is the Digital_Bottom block. All mandatory changes have now been implemented in Verilog.
- Two real bugs in FE-I1 were fixed (PixClk timing and ROC Empty timing error).
- The improvements for SEU-hardening include use of new SEU-latch and SEU-DFF in Command Register and Global Register, duplication of Reset Generator and Address Decoder, generation and checking of Hit Parity, use of SEU-DFF in critical state machines, and use of Hamming code redundancy in the Trigger FIFO.
- The verification and synthesis plus place and route should be completed by no later than Feb 21. Verification of redundant logic is more difficult

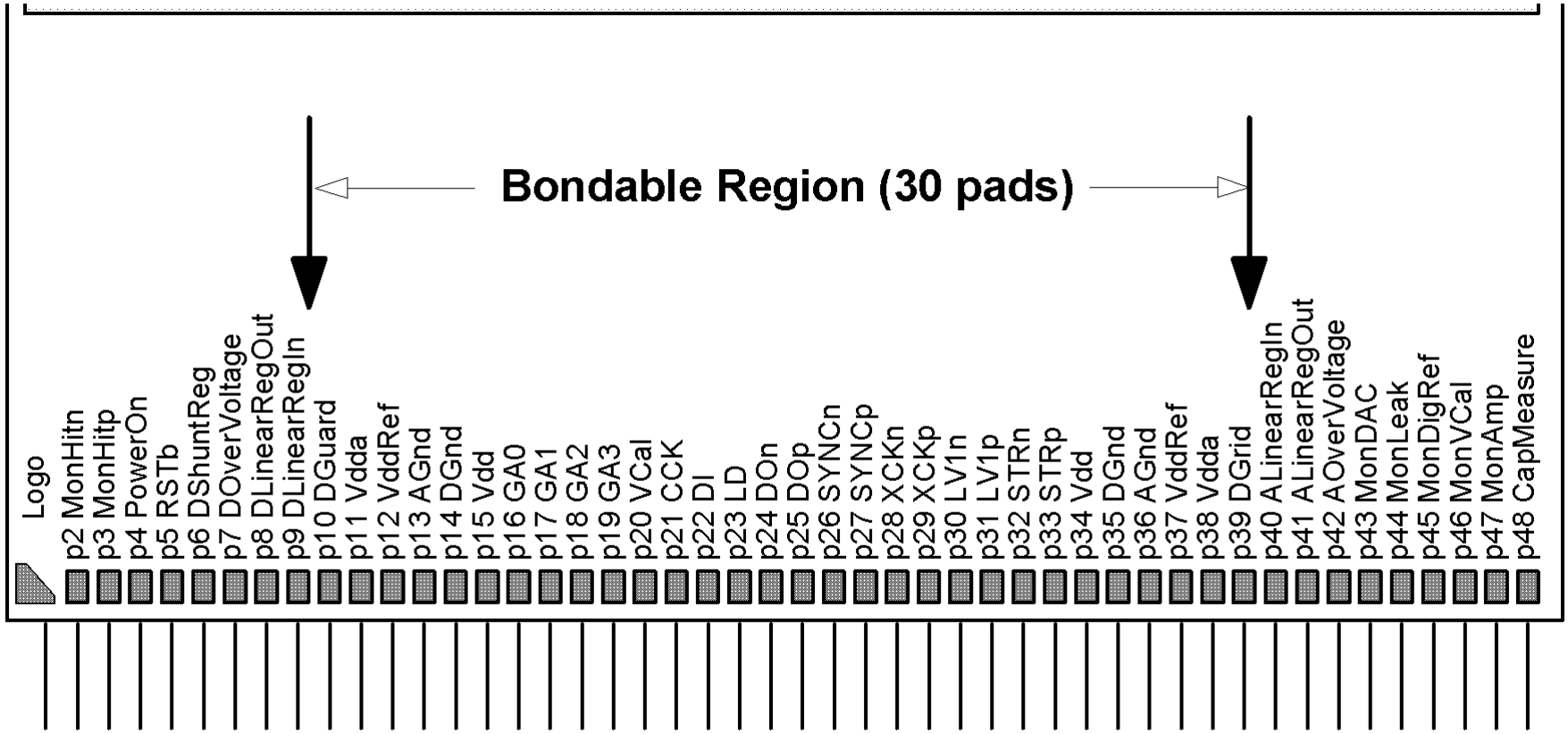
Final Verification:

- In parallel, will begin top-level verification process with “little chip”, consisting of 16-pixel columns and 2-buffer EOC blocks. Once the Digital_Bottom block is placed, the final LVS/DRC checks should begin. This should be completed by Feb 28.

Pinout for FE-I2

Remove two useless pins:

- RefReset pin no longer needed since this is now a Command. CapTest pin is redundant, since there is a Global Register bit for this purpose, and decoupling caps seem to work fine (pin was present in case chip did not power up).
- This allows insertion of a second regulator for the digital supply. This is not a requirement, but could be useful “safety net”. Have also shuffled pads for easier bonding in case regulators or overvoltage protection is needed:



Reticle Layout

- For an IBM run, there is a large area overhead associated with the reticle (test structures), so it should be as large as possible. It must also be easily diced, to minimize chip loss during dicing. These conditions are only satisfied with the present scheme of two FE chips in the reticle.
- In addition, the IBM test structures must be large in one dimension. If we make a reticle with only FE chips, then we end up with a 160μ street and a 400μ street. The 400μ street cannot easily be diced. One saw cut is not wide enough, and two saw cuts so close together will generate lots of silicon debris.
- Therefore, propose to enlarge the smallest possible reticle by 600μ, in order to provide a 1mm dicing street in the direction that requires two saw cuts. This should allow accurate and reliable dicing without greatly increasing the cost of each FE chip.
- This new region will allow test structures of 500μ height to be inserted without intruding into the nominal dicing streets. Propose to include slightly reduced versions of the present AMS and IZM alignment structures. The only chip in the FE-I1 reticle which would fit in this narrow space is the PM bar. However, we have never used this bar with FE-I1, so there is no good argument to include it in FE-I2. IZM has also requested to have a small bumping test structure, which we will include. For now, propose that the only additional designs would be to include regulators as individual chiplets.

Present FE-I2 reticle:

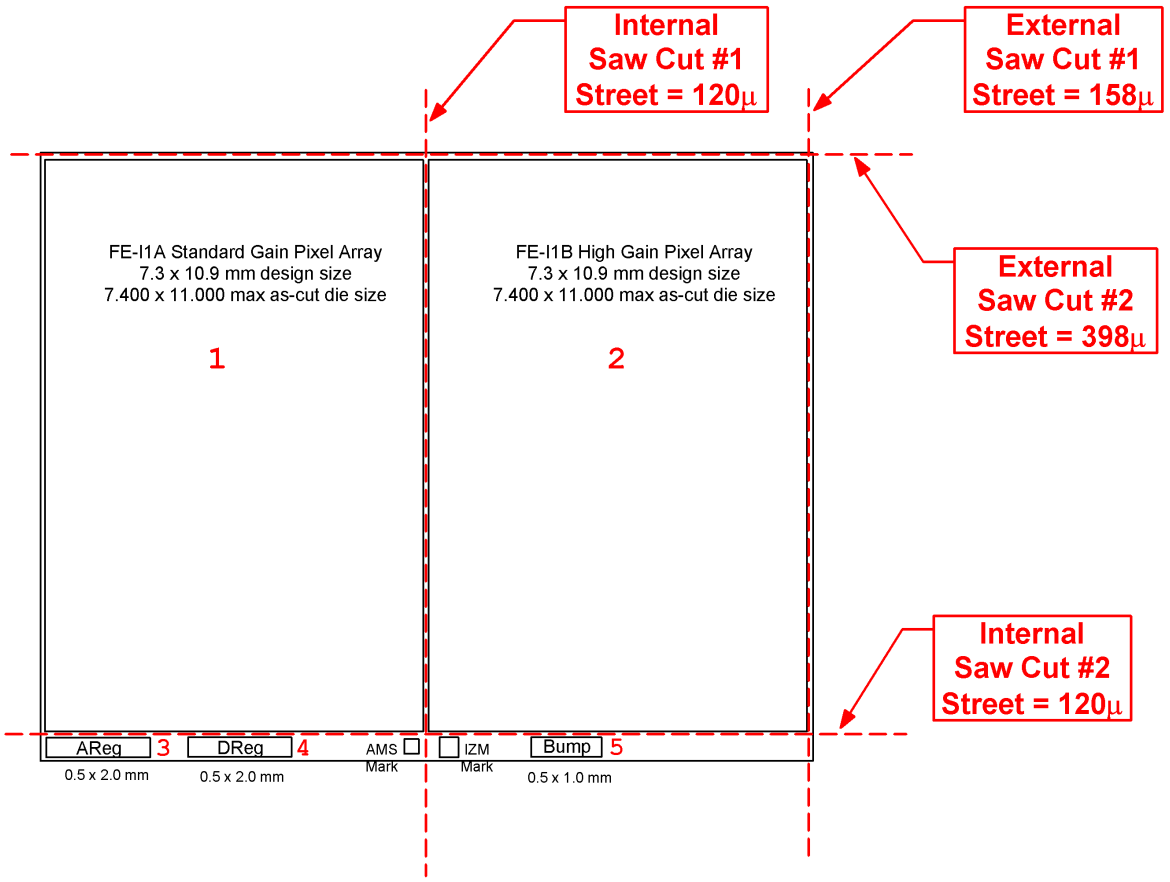
Reticle size is: 14.700 (W) x 11.600 (L) mm

IBM adds 138μ in one direction and 378μ in the other direction.
We choose to have the 138μ added to the left/right of the reticle shown here,
and to have the 378μ added above/below the reticle shown here.

This allows us to meet critical die dimension requirements on Die #1 and #2 with standard dicing procedure.

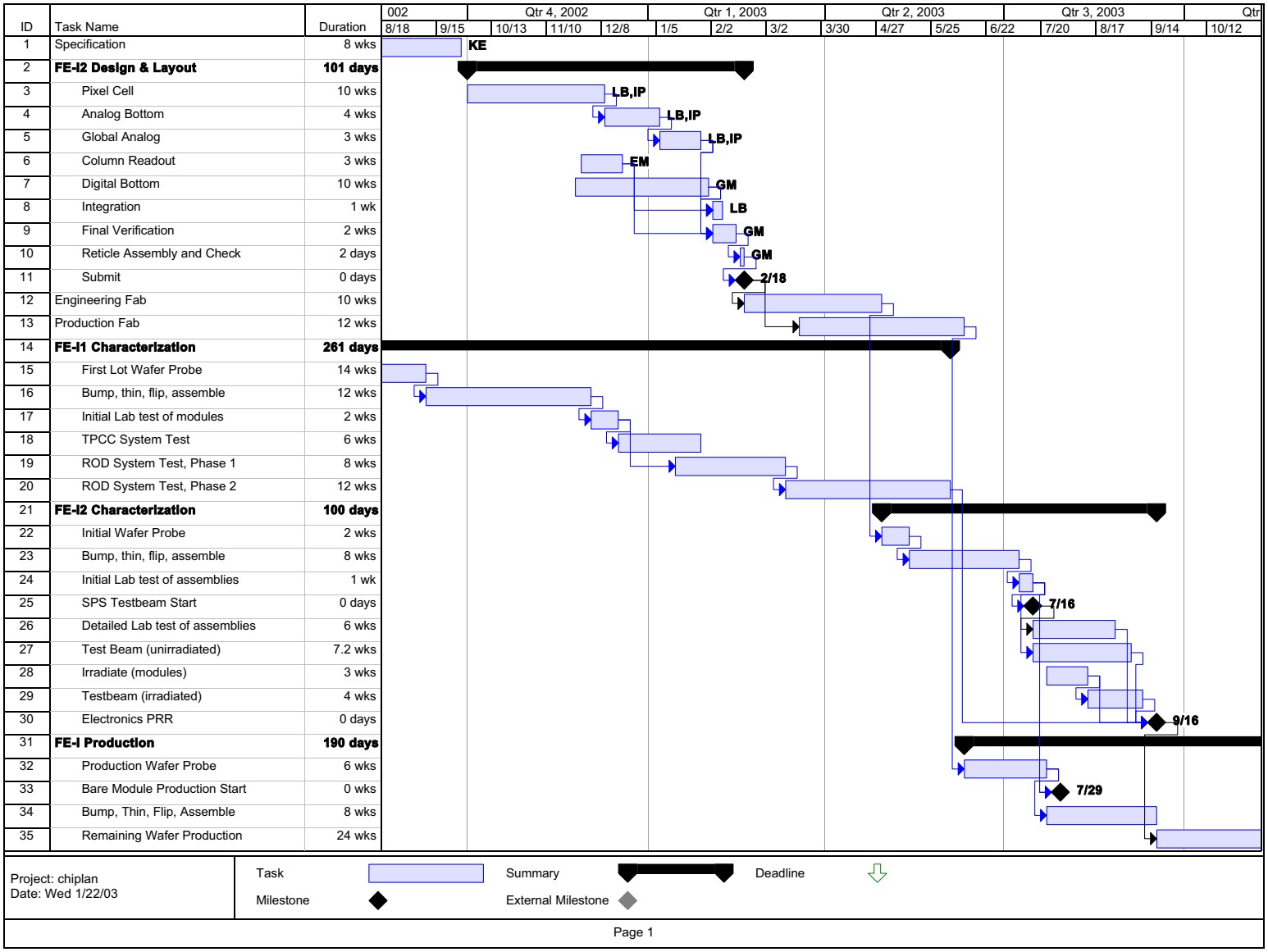
Reticle stepping increments with these rules are: 14.838 (W) x 11.978 (L) mm

Internal Cut #2 and External Cut #2 are separated by only about 1000μ (outer edge to outer edge), so care is required.



Schedule for this year:

- Schedule works backwards from the SPS date (July 17) and the PS date (July23):



ID	Task Name	Duration
1	Specification	8 wks
2	**FE-I2 Design & Layout**	**101 days**
3	Pixel Cell	10 wks
4	Analog Bottom	4 wks
5	Global Analog	3 wks
6	Column Readout	3 wks
7	Digital Bottom	10 wks
8	Integration	1 wk
9	Final Verification	2 wks
10	Reticle Assembly and Check	2 days
11	Submit	0 days
12	Engineering Fab	10 wks
13	Production Fab	12 wks
14	**FE-I1 Characterization**	**261 days**
15	First Lot Wafer Probe	14 wks
16	Bump, thin, flip, assemble	12 wks
17	Initial Lab test of modules	2 wks
18	TPCC System Test	6 wks
19	ROD System Test, Phase 1	8 wks
20	ROD System Test, Phase 2	12 wks
21	**FE-I2 Characterization**	**100 days**
22	Initial Wafer Probe	2 wks
23	Bump, thin, flip, assemble	8 wks
24	Initial Lab test of assemblies	1 wk
25	SPS Testbeam Start	0 days
26	Detailed Lab test of assemblies	6 wks
27	Test Beam (unirradiated)	7.2 wks
28	Irradiate (modules)	3 wks
29	Testbeam (irradiated)	4 wks
30	Electronics PRR	0 days
31	**FE-I Production**	**190 days**
32	Production Wafer Probe	6 wks
33	Bare Module Production Start	0 wks
34	Bump, Thin, Flip, Assemble	8 wks
35	Remaining Wafer Production	24 wks

Project: chiplan
Date: Wed 1/22/03

Task | Summary | Deadline
Milestone | External Milestone

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Basic assumptions for getting to July:

- If submit on Feb 18 (already wrong by almost two weeks), then assume 10 week turnaround for first 6 engineering run wafers. This was turnaround observed for FE-I1, and could be better, but we have no control over this.
- Assume 2 weeks for initial wafer probe. This means the time required to test the FE-I2 design, test the 6 wafers, and send them to the bumping vendors.
- Assume 8 weeks to bump, thin, dice, flip-chip, and assemble modules. Assumes the availability of tested and assembled FlexV5 and MCC-I2 by July 1 (week 27).
- It is possible we should skip thinning steps, as this might save a week (?) This tight schedule will require “hand carrying” wafers to bumpers and very close interaction to assure rapid turnaround (especially with IZM, where processing is more complex). This is the major point where we can compensate for late submission.
- It is critical to start fabrication of FlexV5 and MCC-I2 in a timely way. If we assume 6 week fab time for FlexV5, and 4 weeks for complete test and assembly, it should be submitted by end-March. If we assume 10 week fab time and 2-3 weeks test and dice time for MCC-I2, then this submission must happen by end-March.
- This could allow production of required 12 modules by July 9, allowing one week for characterization. Some modules could come for second SPS week (July 30).
- This is a **VERY CHALLENGING** schedule. It will require constant pushing, but is the only way we can test modules at high intensity, irradiate modules to full dose, and characterize irradiated modules in the testbeam in 2003 !!!